APPLICATION NOTE

AN259

Applications and performance of PTN1111 and PTN2111 clock distribution devices

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2001 Oct 16

Philips Semiconductors

PHILIPS

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INTRODUCTION

The constantly increasing requirements for high-performance level systems have introduced a demand for high-speed, low skew clock generation and distribution networks. Clocks are used to drive processors or to synchronize the data between system components, and consequently, clock distribution networks have become an important part of the system design. Clock skew, which is defined as the time difference between simultaneous clock transitions within a system, can have as much of an impact on the performance of the overall system as any other propagation delay. As speeds are increasing, clock periods are getting shorter, and, hence, skews are becoming more of a problem. These simultaneous demands on skew and speed favor the use of integrated, high-performance, low-skew clock generation devices as the preferred clock distribution strategy.

The PTN1111 and PTN2111 are high-speed, low-skew clock distribution devices, and they have been developed under the Logic Product Group of Philips Semiconductors, targeted mainly for the telecom and networking infrastructure markets. The PTN1111 utilizes PECL as the primary signaling standard, whereas the PTN2111 employs LVDS. Both devices feature low-voltage supply range and high signaling rate capability, and they have been designed, modeled and produced with minimum skew as the key goal. Optimum design and layout served to minimize gate-to-gate skew within the devices, and this resulted in dependable, guaranteed low-skew devices.

PTN1111 and PTN2111 can be used in Network Processor Cards to distribute system clocks across a backplane to multiple line cards; or in Line Cards to distribute a single system clock signal from the backplane to multiple channels on a line card. A trivial clock distribution tree is shown in Figure 1.

In the recent years, differential design was gaining more and more popularity, because of the advantages it provides. The use of differential inputs and outputs in a given ICs makes it less susceptible to electromagnetic interference and noise generation. But the biggest value of the differential design comes in systems, which clocks both off the positive and negative edges.

Both PTN1111 and PTN2111 incorporate the advantages of the differential design.

PTN1111

The PTN1111 has a 1:10 clock distribution ratio, and the clock frequency is 1.5 GHz, and all of the outputs are enabled at all times. The part integrates fully compliant PECL drivers and receivers, and a low voltage supply range of 2.375V to 3.8V. The advantages of PECL go beyond the differential design, because, in general, ECL devices provide superior performance in all areas of skew over their TTL or CMOS competitors, due to their faster propagation delays

PTN2111

The PTN2111 also has a 1:10 clock distribution ratio, operates above 622MHz, and incorporates LVDS I/O. The device can be programmed to turn selected outputs on or off, so either all or selected outputs are running at a particular time. The PTN2111 features two registers — an 11-bit shift register with a serial-in and a control register. The purpose of the control register is to enable or power off each output clock channel and to select the clock input.

The PTN2111 can operate in two modes — programmed mode and standard mode, and this is determined by pin EN-device enable. When EN is LOW, the device is in standard mode of operation and it is not programmable. All clock buffers outputs are enabled, and by toggling the Si pin, the LVDS clock input is selected from either Clock0 or Clock1.

When EN is HIGH, the device is in programmed mode of operation, and the control register is essentially programmed. One way to program the control register is to use an external parallel-in/serial-out register. DIP-switches can be used to assign the D0-D9 + Clk_Sel values. Once those values are set, they could be parallel loaded in the register, and with 12 consecutive clock pulses they would be serially shifted into the Si input of PTN2111, thus determining which clock outputs to be on or off. Setting the EN back to LOW will reset those values. The user should ensure that the setup and hold times of the registers are not violated, as well as that data is clocked in/out on a proper clock edge.

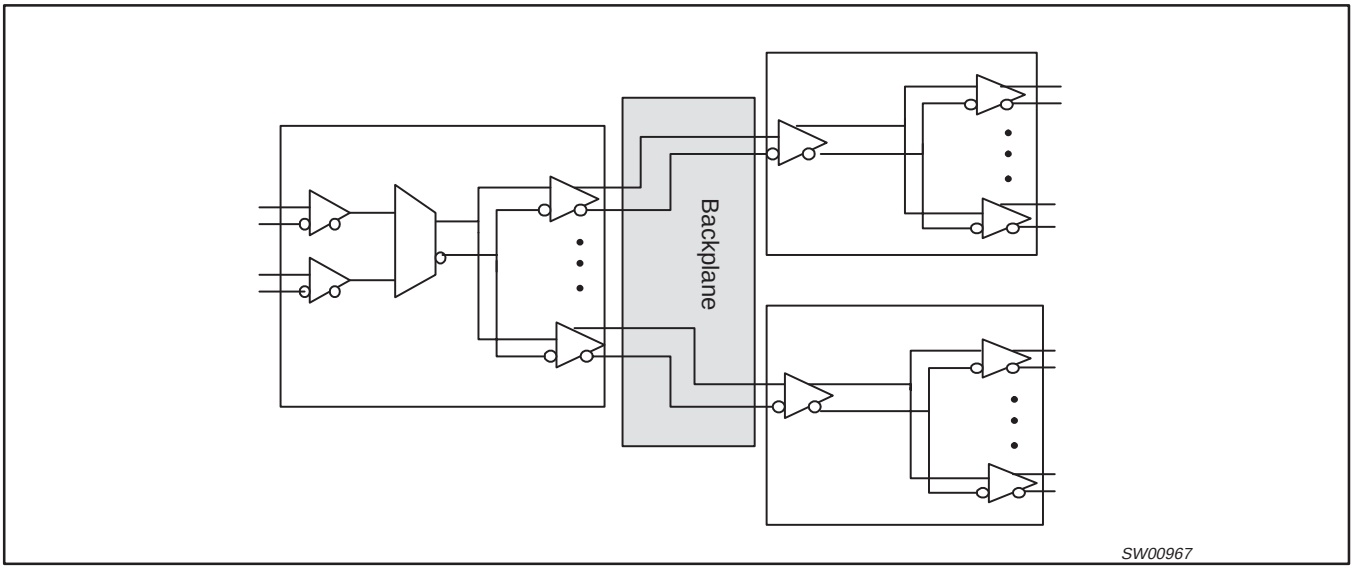

Figure 1. Clock distribution tree

SKEW DEFINITIONS

The main benefit and objective of the design of a clock distribution device is low skew: pulse skew and output-to-output skew, as well as skew measured from part-to-part. For the unfamiliar reader, a brief overview of the clock skew is given below. There are three different types of clock skews — duty cycle, output-to-output, and part-to-part skew, and each of these components are of equal importance, depending on the specific application.

Duty Cycle Skew

Duty cycle or pulse skew is defined as the difference between the TPLH and TPHL propagation delays as shown in Figure 2.

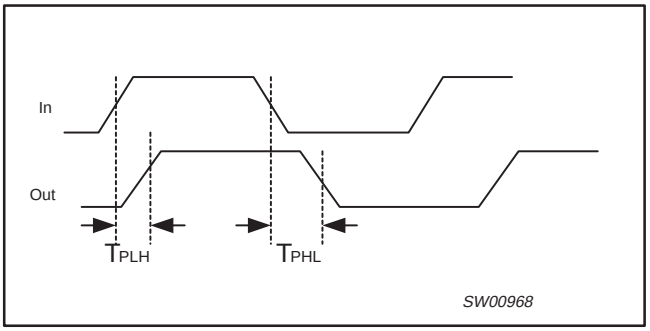

Figure 2. TPLH and TPHL propagation delays

Duty cycle skew, measured on a single output pin, is very important in applications that require timing operations to occur on both edges of the signal, or in systems which use microprocessors and the duty cycle of the input clock signal is very critical.

Under typical conditions, the maximum duty cycle skew for PTN1111 and PTN2111 is specified to be 50ps.

Output-to-Output Skew

Output-to-output skew is a measure of the difference between the propagation delays of the output of the device. It is the difference between the driver's slowest and the driver's fastest output.

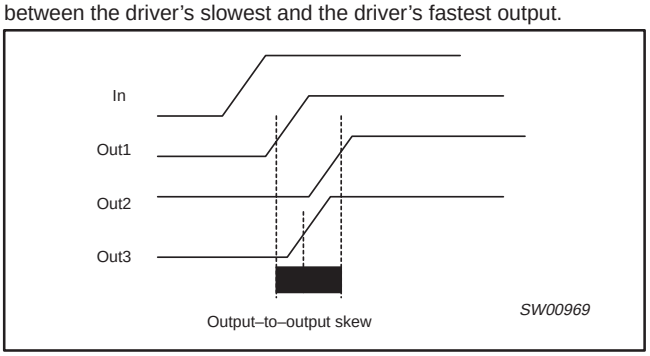

Figure 3.

The output-to-output skew is very important in applications where a single device provides the clock to all other devices in the system or to a clock distribution tree. The ideal situation requires that the output transitions are simultaneous, and if they are not, the output-to-output skew must be added to the duty cycle skew in order to get the total device skew. The output-to-output skew for PTN1111 and PTN2111 is specified to be 35 ps over the commercial operating range.

The major contributor to duty cycle skew and output-to-output skew is the layout of the IC. Thus, a care must be taken when routing the internal paths through the package.

Part-to-Part Skew

The third type of skew is part-to-part or package skew. It is defined as the difference in propagation delay between the slowest output of one device and the fastest output of another device for the same transition. Since the part-to-part skew is dependent on both process and environment variations, the resultant specification is somewhat larger than for the other two components of skew and is by far, the most difficult performance aspect of a device to minimize. The major contributors to variations in propagation delay of silicon devices are power supply and temperature variations.

The power supply aspect applies to situations in which the different outputs of the clock will be distributed on different boards because then there is a real possibility that each device will see different power supply levels. The thermal variations become a problem when devices in various part of the system are under different junction temperature conditions.

The PTN1111's and PTN2111's data sheets specify part-to-part skew to be 100 ps, under assumed equal power supply and temperature conditions.

DESIGN CONSIDERATIONS

Clock skew is an important design consideration in today's high-speed systems, and it must be kept within an acceptable small fraction of the system clock period, if the system is to work successfully and reliably. The skew can be minimized throughout the IC design process by careful circuit design and silicon layout. In general, differences in paths through the package can be minimized regardless of the silicon technology used at the die level. Careful pin configuration can enhance the skew minimization; whereas independent power and ground pins can reduce the ground bounce noise from simultaneously switching outputs. The greatest benefit of the LVDS's and PECL's differential design is that it generates and couples little, if any, noise to the internal power supplies.

The design considerations and efforts go even further because caution must be applied when PTN1111's or PTN2111's outputs are distributed through a PCB. In order to get the maximum performance out of the clock distributor, all the traces and loads must be equalized. The traces must be equal lengths, as short as possible, and without sharp bends or discontinuities.

Since the signals are differential, maintaining differential impedance between two complementary outputs is essential for the signal quality. At the PTN1111's and PTN2111's speed of operations, all traces must be considered as transmission lines and terminated properly in order to prevent any signal integrity issues. PTN2111's LVDS receiver requires the standard 100 Ohms between the two differential input lines. PTN1111's PECL receiver requires an input termination, but the choice is left to the designer. Possible PECL terminations and the standard LVDS termination are shown in Figure 4.

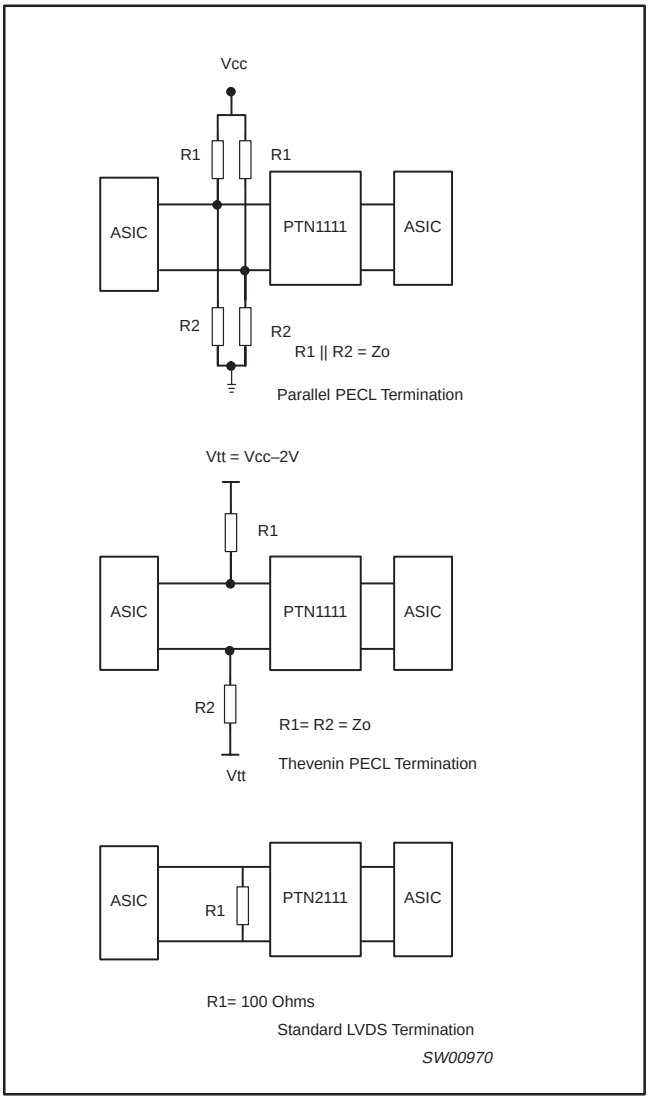

Figure 4.

SKEW MEASUREMENT IN PRACTICE

In order to properly evaluate PTN1111 and PTN2111, whether in house or at the customer's premises, evaluation boards for each IC had been developed. The layouts of the PTN evaluation boards are attached in appendix A for reference, and for further information on the evaluation boards, please, refer to their corresponding application notes.

Coax cables are essential to connect the board (via the SMAs) to the oscilloscope if any measurement or even simple observation of the quality of the signals is to be made. It is important that the SMA cables are the same — i.e. vendor, length, characterization impedance, etc., so there is no extra latency caused by the cables. An oscilloscope and a function generator are necessary for the measurement of the skew of the device. Figure 5 shows a typical test set up for measuring the duty cycle and output-to-output skew:

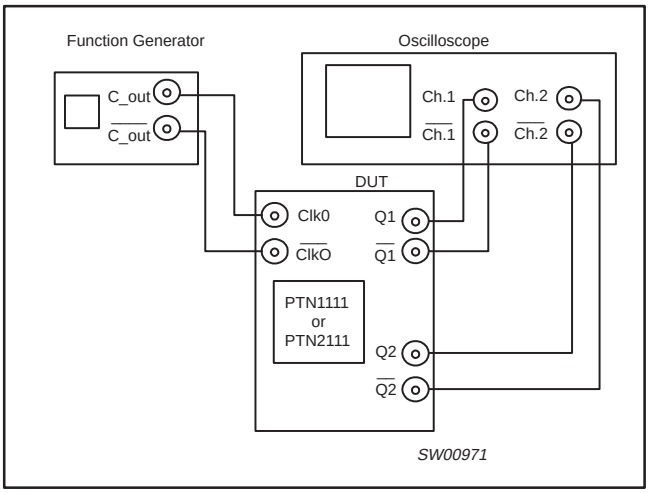

Figure 5.

To measure the duty cycle, valid data must be present at the clock inputs of PTN1111, and one of the clock output is taken for monitoring at the oscilloscope. The duty cycle skew is measured as the timing difference between the two complimentary single ended outputs at their common mode cross over point.

To measure the output-to-output skew, any two outputs of the PTN1111 are fed into the oscilloscope, and by using the scope's build-in measurement features, the difference in propagation delay can be recorded.

CONCLUSION

Thus, PTN1111 and PTN2111 are an excellent solution for systems that need synchronized data or use processors. These clock generator devices are carefully engineered to minimize the skew, thus contributing to reliable and better performance clock distribution systems and are dedicated to simplifying signal integrity challenges. The skew specification of both devices gives the designers the freedom to control the skew at each phase of their design, which simplifies the challenge of meeting over all system requirements.

REFERENCES

Wakerly, John. *Digital Design: Principles and Practice*, 2nd edition, 1995 Prentice Hall, Inc.

High Performance ECL Data, second edition. Motorola Inc., 1995

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Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 10-01

Document order number: 9397 750 08979

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